

ARRAY SUBSTRATE AND METHOD OF FABRICATING THE SAME

This present patent document is a divisional of U.S. patent application Ser. No. 13/966,507, filed Aug. 14, 2013 which claims the benefit of Korean Patent Application No. 10-2012-0142875, filed in Korea on Dec. 10, 2012, which is incorporated by reference in its entirety.

BACKGROUND

1. Field of the Disclosure

The present disclosure relates to an array substrate, and more particularly, to an array substrate and a method of fabricating the same.

2. Discussion of the Related Art

Recently, with the advent of an information-oriented society, the field of display devices configured to process and display a large amount of information has rapidly been developed. In particular, liquid crystal displays (LCDs) or organic light emitting diodes (OLEDs) have lately been developed as flat panel displays (FPDs) having excellent performance, such as a small thickness, light weight, and low power consumption, and has superseded conventional cathode-ray tubes (CRTs).

Among LCDs, an active matrix (AM)-type LCD including an array substrate having a TFT serving as a switching element capable of controlling on/off voltages of each of pixels may have excellent resolution and capability of embodying moving images.

FIG. 1 is a cross-sectional view illustrating a pixel region including a thin film transistor in an array substrate of an LCD or an OLED according to the related art.

As shown in FIG. 1, a plurality of gate lines (not shown) and a plurality of data lines 33 cross each other on an array substrate 11 to define a plurality of pixel regions P. A gate electrode 15 is formed in a switching region TrA of each pixel region P. A gate insulating layer 18 is formed entirely on the gate electrode 15, and a semiconductor layer 28 including an active layer 22 of intrinsic amorphous silicon and an ohmic contact layer 26 of impurity-doped amorphous silicon is formed on the gate insulating layer 18.

A source electrode 36 and a drain electrode 38 are formed on the ohmic contact layer 26 corresponding to the gate electrode 15 and spaced apart from each other. The gate electrode 15, the gate insulating layer 18, the semiconductor layer 28, and the source and drain electrodes 36 and 38, which are sequentially stacked at the switching region TrA, forms a thin film transistor Tr.

Furthermore, a passivation layer 42 including a drain contact hole 45 and exposing the drain electrode 38 is formed entirely on the source and drain electrodes 36 and 38. A pixel electrode 50 is formed in each of pixel regions P on the passivation layer 42 and contacts the drain electrode 38 through the drain contact hole 45. A semiconductor pattern 29 is formed below the data line 33 and has a double-layered structure of first and second patterns 27 and 23, which are made of the same materials as the ohmic contact layer 26 and the active layer 22, respectively.

In the semiconductor layer 28 of the thin film transistor Tr formed in the switching region TrA, the active layer 22 has a first thickness t1 where the ohmic contact layer 26 is formed and has a second thickness t2 where the ohmic contact layer 26 is removed and exposed. This difference in thickness is caused by a fabrication method, and since the thickness is reduced at the portion exposed between the

source and drain electrodes 36 and 38, property of the thin film transistor Tr is degraded.

To solve this problem, a thin film transistor shown in FIG. 2 is developed, which does not need an ohmic contact layer and has a single-layered oxide semiconductor layer 79.

FIG. 2 is a cross-sectional view illustrating a pixel region of an array substrate including a thin film transistor having an oxide semiconductor layer according to the related art.

Referring to FIG. 2, a thin film transistor Tr includes a gate electrode 73 on a substrate 71, a gate insulating layer 75, an oxide semiconductor layer 77, source and drain electrodes 81 and 83, and an etch stopper 79. A passivation layer 85 is on the transistor Tr and has a drain contact hole 87 exposing the drain electrode 83. A pixel electrode 89 is on the passivation layer 85 and contacts the drain electrode 83 through the drain contact hole 87.

Since the ohmic contact layer is not needed, the oxide semiconductor layer 77 is not required to be exposed in a dry-etching, which is performed to form the ohmic contact layers of impurity-doped amorphous silicon spaced apart from each other, and degradation of property of thin film transistor Tr can be prevented.

Further, carrier mobility of the oxide semiconductor layer 77 is a several times to a ten times greater than that of the semiconductor layer using the amorphous silicon, and it is advantageous to a driving transistor.

However, when the oxide semiconductor layer 77 is exposed to an etching solution to pattern a metal layer, the oxide semiconductor layer 77 is removed because of no etch selectivity with the metal layer or causes degradation of property of the thin film transistor Tr because of damage to molecule structure of the oxide semiconductor layer 77.

Further, when the oxide semiconductor layer 77 is exposed to an etching solution, reliability of operation of the thin film transistor Tr is degraded, and particularly, variation rate of threshold voltage greatly changes as time passes in a BTS (bias temperature stress) test, and thus property distribution or divergence in display region is great, and thus display quality is adversely affected.

To solve the problems, in order that a center portion of the semiconductor layer 77 i.e., a channel portion, is not exposed to an etching solution which reacts with a metal material for the source and drain electrodes 81 and 83 in a patterning process of forming the source and drain electrodes 81 and 83, an etch stopper 79 made of inorganic insulating material is formed on the center portion of the semiconductor layer 77.

However, the array substrate 71 including the thin film transistor Tr having the oxide semiconductor layer and the etch stopper 79 needs margin to contact between the oxide semiconductor layer 77 and the source and drain electrodes 81 and 83 because of the etch stopper 79. Accordingly, the source and drain electrodes 81 and 83 needs to be formed relatively long, and thus overlapping area with the gate electrode 73 increases and parasitic capacitance increases. Further, one mask process is required to form the etch stopper 79, and thus the array substrate is fabricated with six (or five) mask processes.

The mask process includes five steps of a photoresist deposition, a light exposure, a developing, an etching and a stripping, and thus the mask process is complicated and requires many solutions. Accordingly, as a number of the mask process increases, production time increases and production rate decreases, error rate increases, and production cost increases.